LH5324A00

CMOS 24M (1.5M × 16) Mask-Programmable ROM

FEATURES

- 1,572,864 words × 16 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 357.5 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package: 42-pin, 600-mil DIP

DESCRIPTION

The LH5324A00 is a 24M-bit mask-programmable ROM organized as 1,572,864 × 16 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

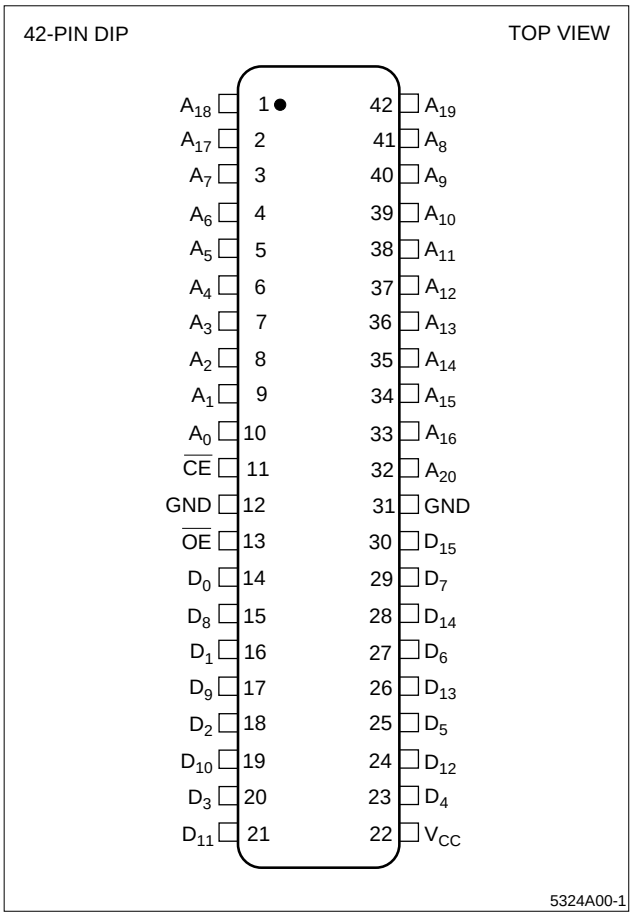


Figure 1. Pin Connections for DIP Package

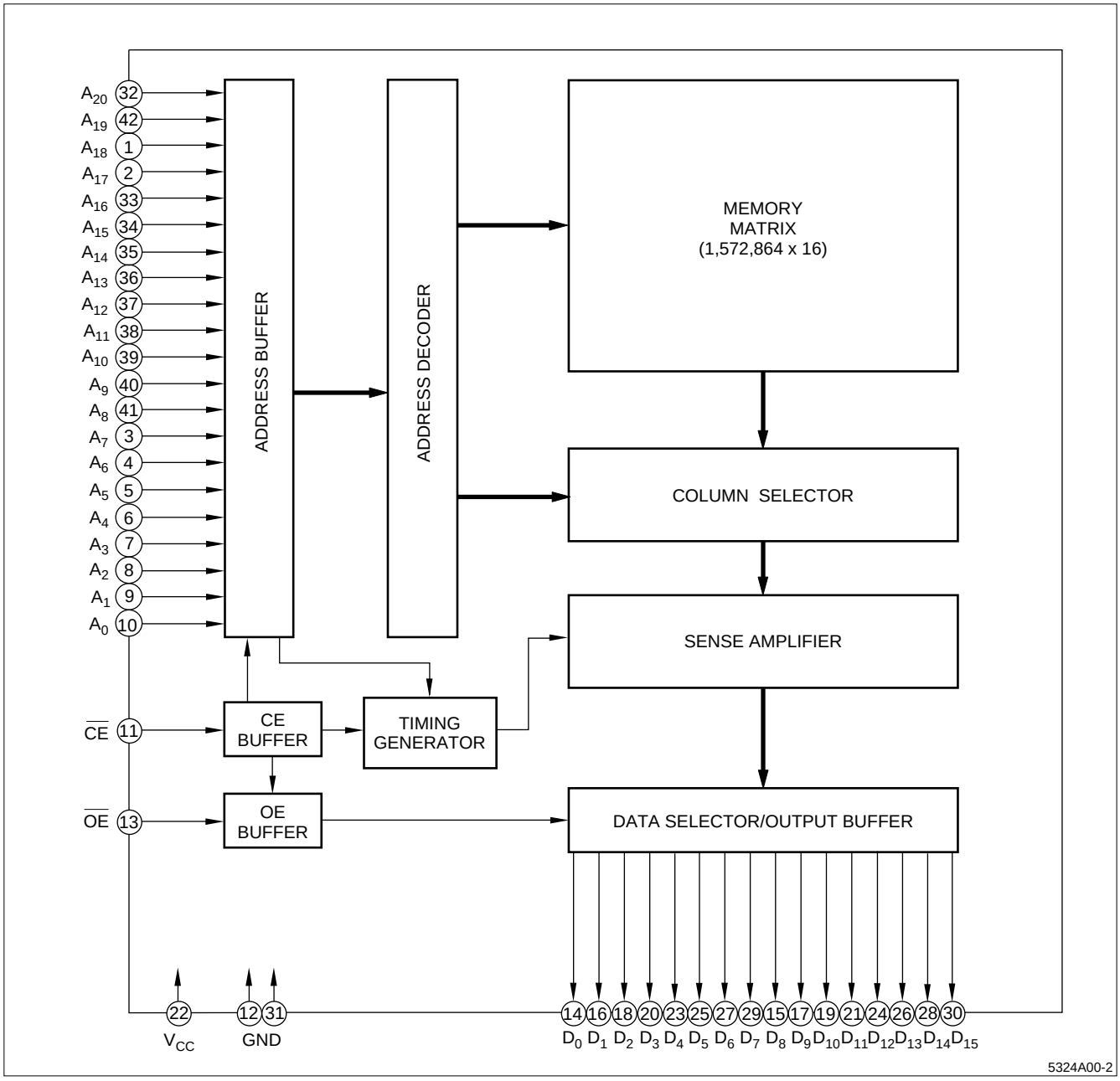


Figure 2. LH5324A00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
$A_0 - A_{20}$	Address input
$D_0 - D_{15}$	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	OE	$A_0 - A_{18}$	A_{19}	A_{20}	DATA OUTPUT $D_0 - D_{15}$	SUPPLY CURRENT	NOTE
H	X	X	X	X	High-Z	Standby (I_{SB})	1
L	H	X	X	X	High-Z	Operating (I_{CC})	1
L	L	X	L	L	Output	Operating (I_{CC})	1
L	L	X	L	H	Output	Operating (I_{CC})	1
L	L	X	H	L	Output	Operating (I_{CC})	1
L	L	X	H	H	Unspecified	Operating (I_{CC})	1, 2

NOTE:

1. X = H or L; High-Z = High-impedance
2. When the address input at both A_{19} and A_{20} is high level, outputs become high-impedance irrespective of $\overline{CE}$ or $\overline{OE}$.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		–0.3	0.8	V	
Output 'High' voltage	V_{OH}	I_{OH} = –400 µA	2.4		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		65	mA	2
	I_{CC2}	t_{RC} = 1 µs		55		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz		10	pF	
Output capacitance	C_{OUT}	T_A = 25°C		10	pF	

NOTES:

1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable access time	t_{ACE}		150	ns	
Output enable delay time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
Output floating time	t_{CHZ}		60	ns	1
	t_{OHZ}		60	ns	
	t_{AHZ}		70	ns	

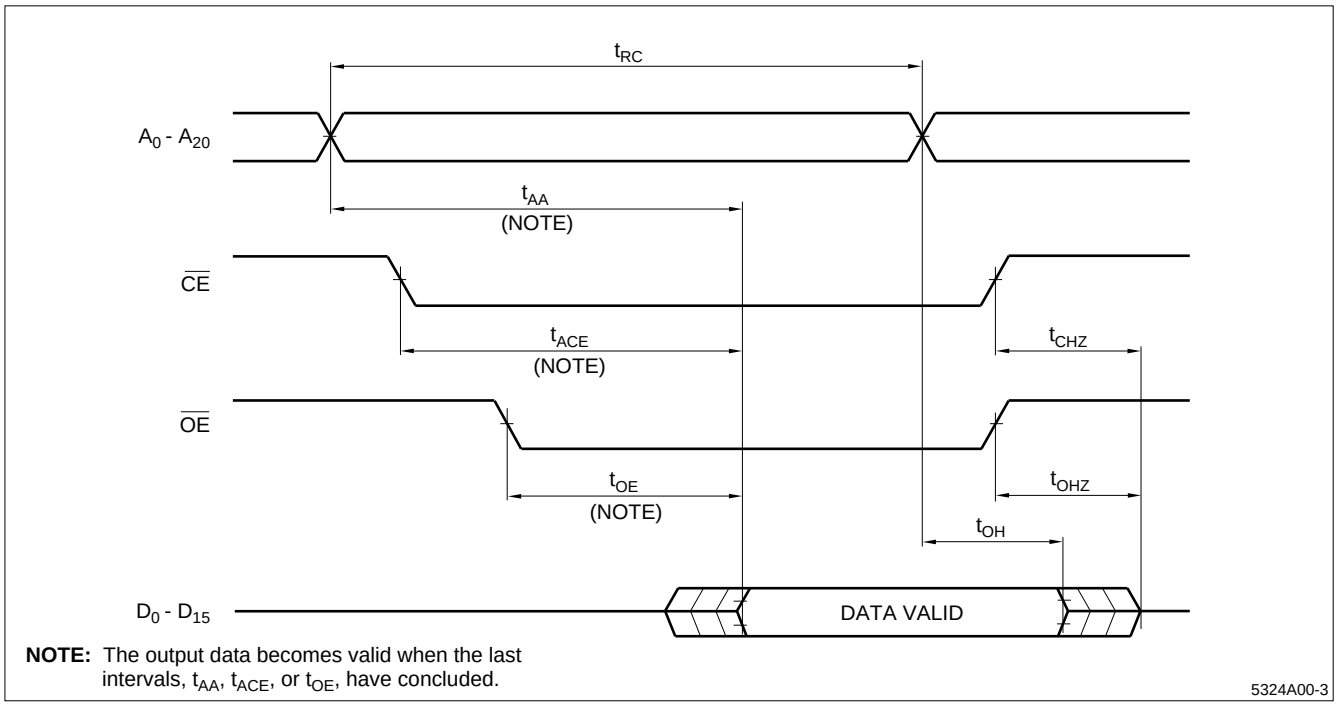
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input signal rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

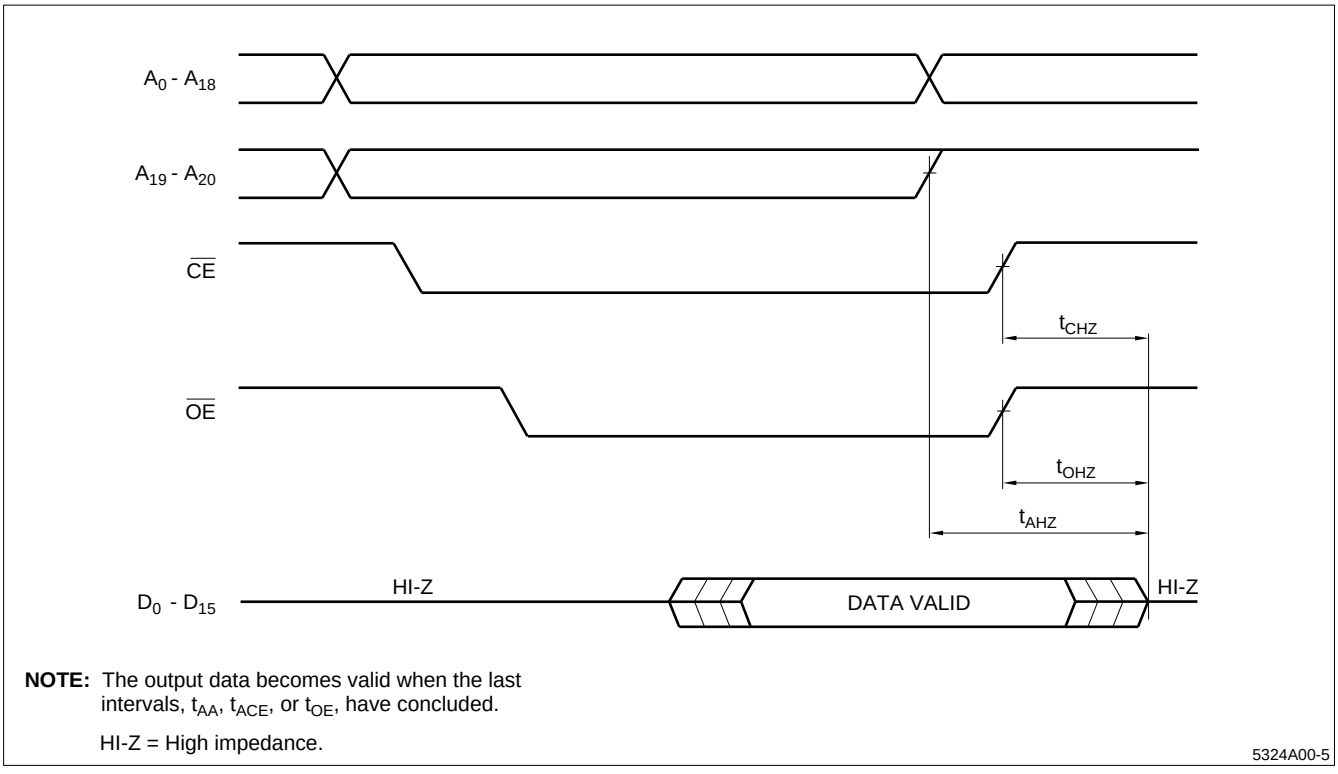
CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

Figure 3. Timing Chart

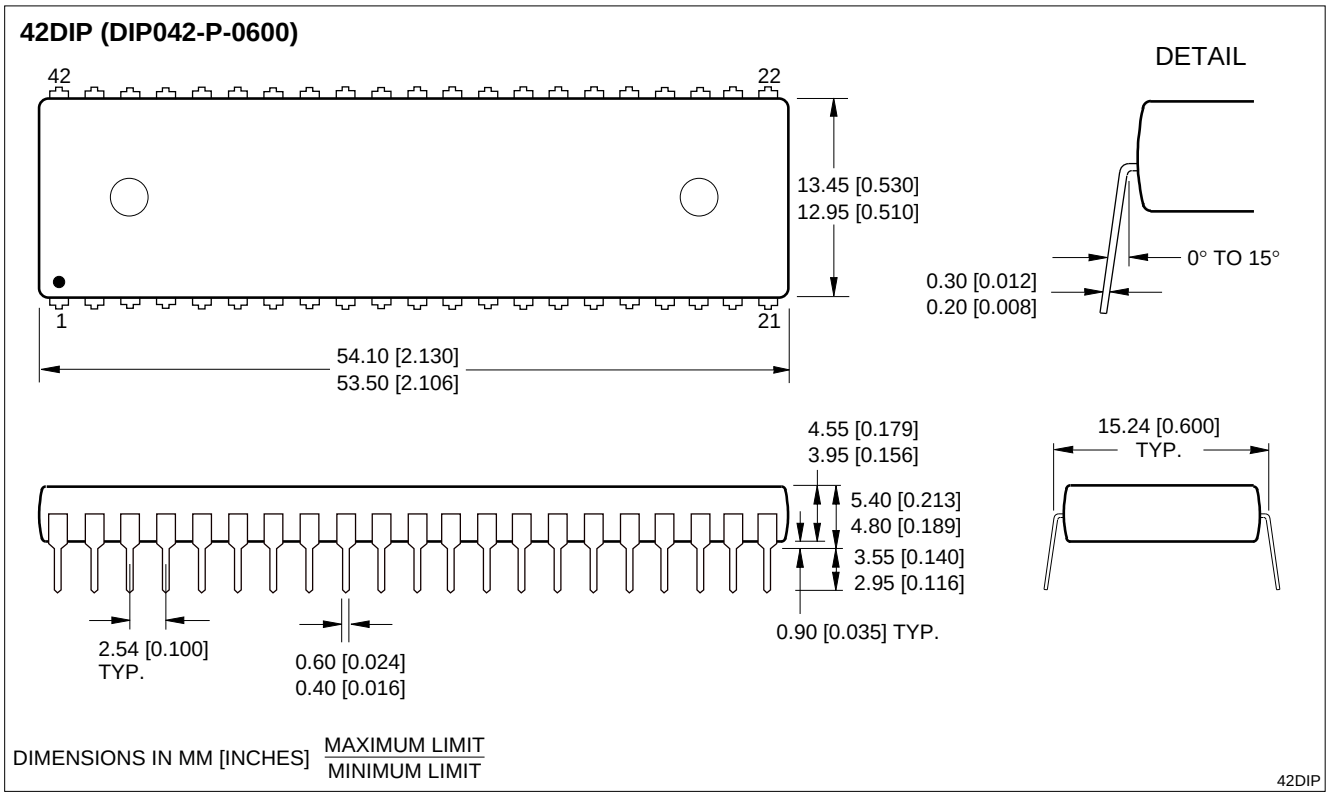


NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

HI-Z = High impedance.

Figure 4. Timing Chart (When the Address Input at Both A_{19} and A_{20} High Level)

PACKAGE DIAGRAM



42-pin, 600-mil DIP

ORDERING INFORMATION